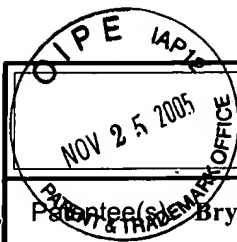


09/ 886823

Cofc



**TRANSMITTAL LETTER**  
(General - Patent Issued)

Docket No.  
BUR920000059US1

Patentee(s) Bryant et al.

U.S. Patent No.

6,960,806 B2

Issue Date

November 1, 2005

Title: **DOUBLE GATED TRANSISTOR AND METHOD OF FABRICATION**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Certificate of Correction  
Postcard

**Certificate**  
**NOV 30 2005**  
**of Correction**

No fee required below. Errors were made by the U.S. Patent Office.

- ☒ No additional fee is required.
- ☐ A check in the amount of \_\_\_\_\_ is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account 09-0456 (IBM) as described below.
- ☐ Charge the amount of \_\_\_\_\_
- ☒ Credit any overpayment.
- ☒ Charge any additional fee required.
- ☐ Payment by credit card. Form PTO-2038 is attached.

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

*Jack P. Friedman*  
Signature

Dated: 11-21-2005

Jack P. Friedman, Ph.D.  
Reg. No. 44,688  
Schmeiser, Olsen & Watts  
3 Lear Jet Lane, Suite 201  
Latham, NY 12110  
(518)220-1850

Customer No.: 30449

CC:

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on

11-21-2005

(Date)

*Betty Zuelsdorf*  
Signature of Person Mailing Correspondence

Betty Zuelsdorf

Typed or Printed Name of Person Mailing Correspondence

NOV 30 2005

P17A/REV04

# UNITED STATES PATENT AND TRADEMARK OFFICE

## CERTIFICATE OF CORRECTION

PATENT NO. : 6,960,806 B2

DATED : November 1, 2005

INVENTOR(S) : Bryant et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

**Page 1, in the Title**

Delete "DOUBLE GATED VERTICAL TRANSISTOR WITH DIFFERENT FIRST AND SECOND GATE MATERIALS" and insert --DOUBLE GATED TRANSISTOR AND METHOD OF FABRICATION--

**Column 1**

Lines 1-3, delete "DOUBLE GATED VERTICAL TRANSISTOR WITH DIFFERENT FIRST AND SECOND GATE MATERIALS" and insert --DOUBLE GATED TRANSISTOR AND METHOD OF FABRICATION--

**Column 11**

Line 53, delete "n-type" and insert --p-type--

Line 58, delete "tho" and insert --the--

**Column 12**

Line 9, delete "or claim 8" and insert --of claim 8--

Line 34, delete "a first safe" and insert --a first gate--

MAILING ADDRESS OF SENDER (Please do not use customer number)

Jack P. Friedman, Ph.D.  
Reg. No. 44,688  
Schmeiser, Olsen & Watts  
3 Lear Jet Lane, Suite 201  
Latham, NY 12110

PATENT NO. 6,960,806 B2

No. of additional copies



NOV 30 2005